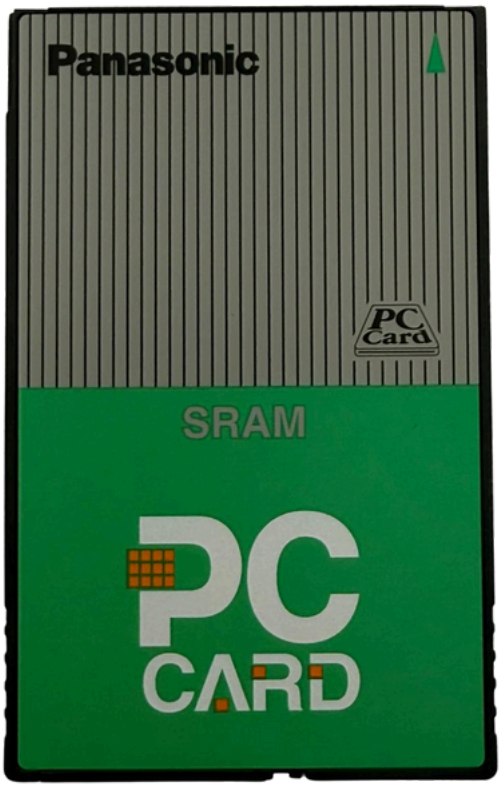
JEIDA Ver.4.2/PCMCIA Rel.2.1 SRAM Card
PRODUCT SPECIFICATION

Model # : BN-064HSR(C)
BN-128HSR(C)
BN-256HSR(C)
BN-512HSR(C)
BN-01MHSR(C)
BN-02MHSR(C)
BN-04MHSR(C)
BN-08MHSR(C)



Contents

1. Scope

This products specification relates to the Panasonic SRAM Card BN-HSR series. This SRAM Card conforms to updated Release 2.1 of PC Card standard specification which has been studied by Personal Computer Memory Card International Association (PCMCIA).

2. Products Model

Table 1 Products Model #

Model #	Common Memory		Attribute Memory		Battery	
	Configuration (Word×bit)	Size (byte)	Configuration	Size (byte)	Main Battery	Sub Battery
BN-064HSR	64K×8 / 32K×16	64K	FF Output	No Memory	CR2025 Lithum Battery	Rechargable Battery
BN-128HSR	128K×8 / 64K×16	128K				
BN-256HSR	256K×8 / 128K×16	256K				
BN-512HSR	512K×8 / 256K×16	512K				
BN-01MHSR	1M×8 / 512K×16	1M				
BN-02MHSR	2M×8 / 1M×16	2M				
BN-04MHSR	4M×8 / 2M×16	4M				
BN-08MHSR	8M×8 / 4M×16	8M				
BN-064HSRC	64K×8 / 32K×16	64K	2K×8	2K		
BN-128HSRC	128K×8 / 64K×16	128K				
BN-256HSRC	256K×8 / 128K×16	256K				
BN-512HSRC	512K×8 / 256K×16	512K				
BN-01MHSRC	1M×8 / 512K×16	1M				
BN-02MHSRC	2M×8 / 1M×16	2M				
BN-04MHSRC	4M×8 / 2M×16	4M				
BN-08MHSRC	8M×8 / 4M×16	8M				

3. Outline

3.1. Physical Specification

Table 2 Physical Specification

Length	85.6±0.2 mm
Width	54.0±0.1 mm
Thickness	3.3±0.1 mm
Pin counts	68 pins

3.2. Temperature Condition

Table 3 Temperature Condition

Parameters	Symbol	Minimum	Maximum	Unit
Operation Temperature	TOPT	0	60	℃
Storage Temperature	TSTG	-20	70	℃

4. Pin Assignment

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	GND	18	VPP1	35	GND	52	VPP2
2	D3	19	A16	36	CD1#	53	A22
3	D4	20	A15	37	D11	54	A23
4	D5	21	A12	38	D12	55	A24
5	D6	22	A7	39	D13	56	A25
6	D7	23	A6	40	D14	57	VS2#
7	CE1#	24	A5	41	D15	58	RESET
8	A10	25	A4	42	CE2#	59	WAIT#
9	OE#	26	A3	43	VS1#	60	RFU
10	A11	27	A2	44	RFU	61	REG#
11	A9	28	A1	45	RFU	62	BVD2
12	A8	29	A0	46	A17	63	BVD1
13	A13	30	D0	47	A18	64	D8
14	A14	31	D1	48	A19	65	D9
15	WE#	32	D2	49	A20	66	D10
16	READY	33	WP	50	A21	67	CD2#
17	VCC	34	GND	51	VCC	68	GND

5. Pin Definition

A0 - A25 Address input pins; Up to 64Kbyte memory space is supported. A25 is the most significantbit and A0 is the least significant bit. Address input pins exceeding its memory size are not connected in the card and are full-decoded in each memory space.
D0 - D15 Data I/O pins; D15 is the most significant bit and D0 is the least significant bit.
CE1#,CE2# Card Enable input pins; -CE1 controls even byte and -CE2 does odd byte. Both of them can be accessed on D0 - D7 by combination of A0, CE1# and CE2#.
WE# Write Enable input pin; This signal controls the write operation to the card.
OE# Output Enable input pin; This signal controls the read operation from the card.
REG# Attribute Memory Select input pin; When the low level assertion of this signal, the attribute memory space is enable.
READY Ready/ Busy output pin; This signal is NC (Not Connected with any card circuitry).
WP Write Protect output pin; WP is at high level during write protection and low level during write enable. This signal reflects write protection status in both common and attribute memory.
CD1#,CD2# Card Detection signal output pins; These output GND level and detect insertion or removal of the card. When they are pulled up to VCC at the system side, the insertion or removal of the card can be detected as digital signals through the buffer.
VS1#,VS2# Voltage Sense output pins; These signals are prepared to check whether the supported power supply voltage is 3.3 V or 5.0 V. In this card, both are NC indicates 5.0 V only supported. In order to apply this status at the system, the host must have pulled-up registor from 10 KΩ to 100 KΩ on socket.
BVD1,BVD2 Battery Voltage Detection output pins
RESET Reset input pin; This signal is NC in this card.
WAIT# Wait output pin; This signal is NC in this card.
RFU Reserved for Future Use pins; This signal is NC in this card.
VCC Power supply pin; In this card, This signal is for +5V.
VPP1,VPP2 Peripheral power supply pins; these signals are NC in this card.
GND Ground pins 0V

6. Bias Power Supply Condition

6.1. Absolute Maximum Rating

Table 5 Absolute Maximum Rating

Parameters	Symbol	Minimum	Maximum	Unit
Power Supply Voltage	VCC	0	6	V
Input Voltage	VI	-0.5	VCC+0.5	V

6.2. Recommended Operation Condition

Table 6 Recommended Operation Condition

Parameters	Symbol	Minimum	Typical	Maximum	Unit
Power Supply Voltage	VCC	4.5	5.0	5.5	V
High Level Input Voltage	VIH	2.2		VCC	V
Low Level Input Voltage	VIL	0		0.8	V

7. Truth Table

7.1. Common Memory Read Operation

Table 7 Common Memory Read Operation

Function Mode	REG#	CE2#	CE1#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby Mode	X	H	H	X	X	X	Hi-z	Hi-z
Byte Access (8 bit)	H	H	L	L	L	H	Hi-z	Even Byte
	H	H	L	H	L	H	Hi-z	Odd Byte
Word Access (16 bit)	H	L	L	X	L	H	Odd Byte	Even Byte
Odd-Byte-Only Access	H	L	H	X	L	H	Odd Byte	Hi-z

Note X: can be either High level input or Low level input
H: stands for High level input, L: stands for Low level input
Hi-z: stands for High impedance

7.2. Common Memory Write Operation

Table 8 Common Memory Write Operation

Function Mode	REG#	CE2#	CE1#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby Mode	X	H	H	X	X	X	Hi-z	Hi-z
Byte Access (8 bit)	H	H	L	L	H	L	Not Valid	Even Byte
	H	H	L	H	H	L	Not Valid	Odd Byte
Word Access (16 bit)	H	L	L	X	H	L	Odd Byte	Even Byte
Odd-Byte-Only Access	H	L	H	X	H	L	Odd Byte	Not Valid

8. DC Characteristics

8.1. General Characteristics

Table11 GeneralCharacteristics

VCC=5.0V±10%, Ta=0℃～60℃

Parameter	Symbol	TestCondition	Value			Unit
			Min.	Typ.	Max.	
Active Current	ICC1	VCC=VCC Max.,CE1# or CE#2=VIL tCR=200ns, IOUT=0mA			80	mA
	ICC2 ISB	VCC=VCC Max.,CE1#=CE#2=VIL tCR=200ns, IOUT=0mA			150	mA
Standby Current		VCC=VCC Max.,CE1#=CE#2=VIH Empty charged toSubBattery			5	mA
		VCC=VCC Max.,CE1#=CE#2=VIH Full charged toSubBattery VCC=VCC Max.,VIN=VCCorGND		100	150	μA
Input Leakage Current	I_{LI}	VCC=VCC Max.,VOUT=VCCor			± 10	μA
Output Leakage Current	I^{LO}	GND			± 10	μA
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH}		2.2		VCC	V
Output Low Voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA	3.8			

8.2. Capacitance

Table 12 Capacitance

(Ta=25℃, f=1.0MHz, not 100% tested)

	Symbol	Maximum Value	Unit
Address signals /Control Signals	$C_{I/O}^{IN}$	100	pF
Data signals	C	50	pF

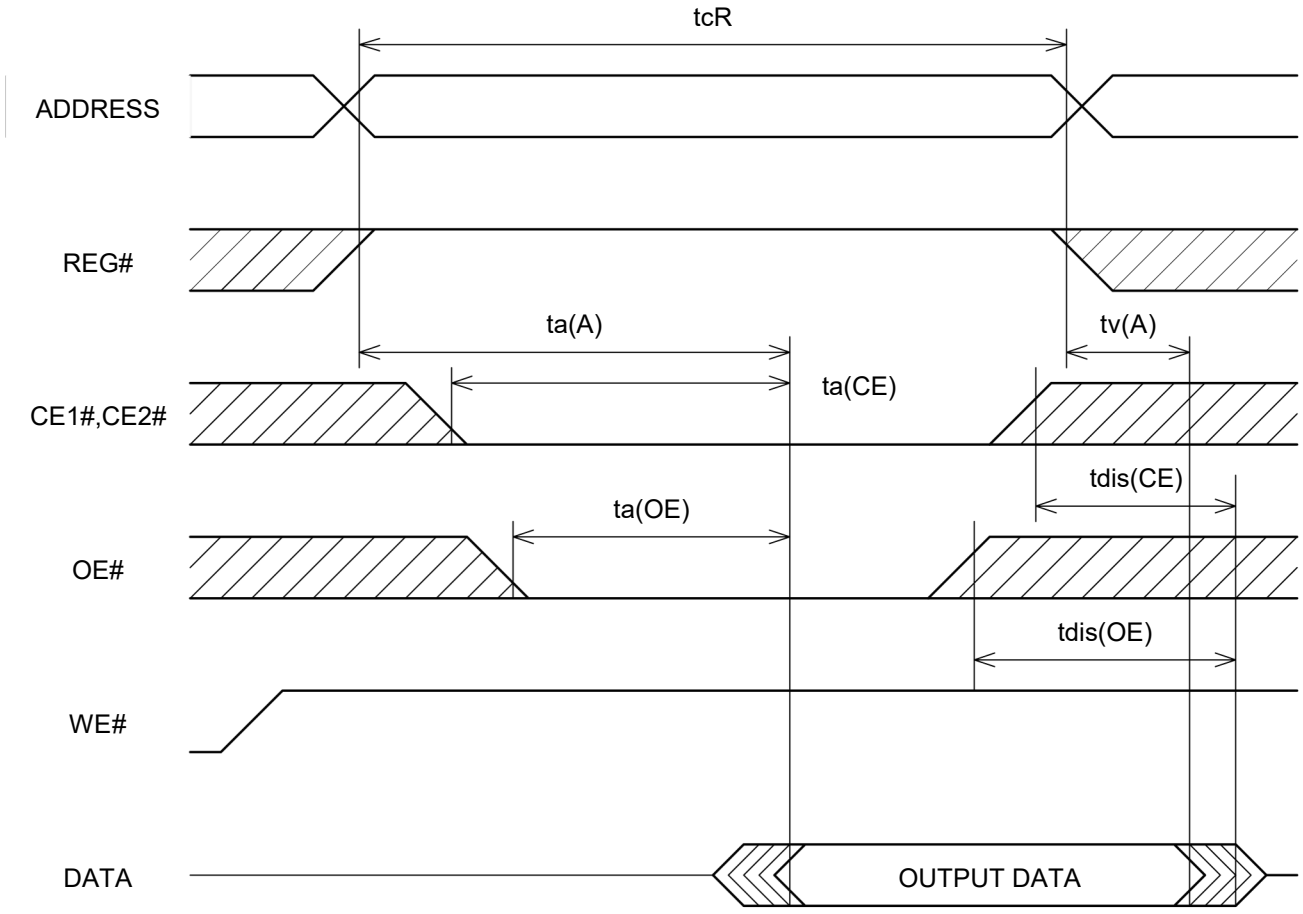
9. AC Characteristics

9.1. Read Cycle Timing (for Common memory and Attribute memory)

Table 14 Read Cycle Timing (for Common memory and Attribute memory)

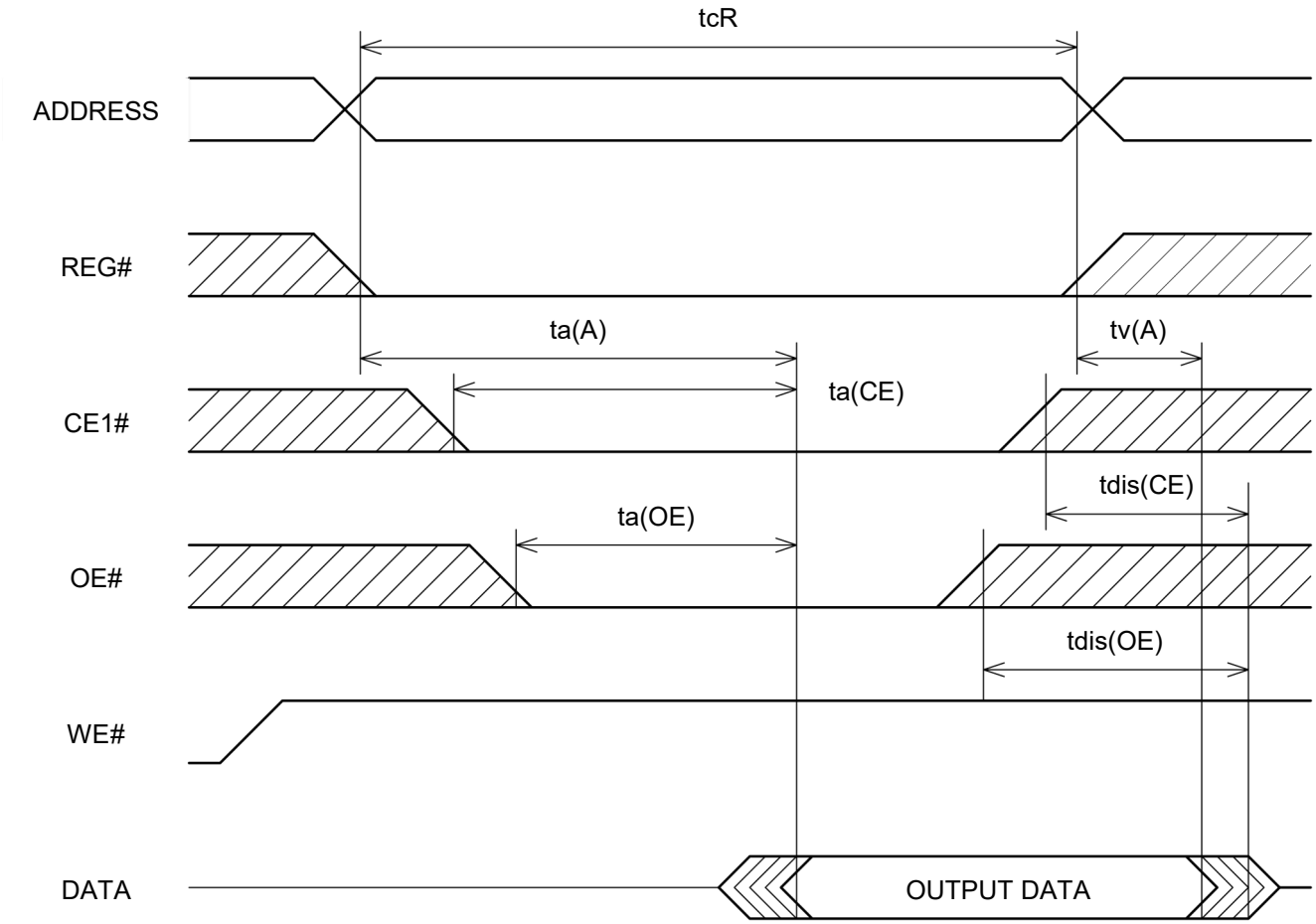
VCC=5V±10%, Ta=0℃～60℃

Parameter	Symbol	Common Memory		Attribute Memory		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	tCR	200		300		ns
Address Access Time	ta(A)		200		300	ns
CE# Access Time	ta(CE)		200		300	ns
OE# Access Time	ta(OE)		100		150	ns
Output Disable Time from CE# Change	tdis(CE)		90		100	ns
Output Disable Time from OE# Change	tdis(OE)		90		100	ns
Output Enable Time from CE# Change	ten(CE)	5		5		ns
Output Enable Time from OE# Change	ten(OE)	5		5		ns
Data Valid Time from Address Change	tv(A)	0		0		ns



Note) 1. Shaded sections denote areas where the level can be either high or low.
2. Output load : 1TTL + 100pF

Figure 1 Common Memory Read Cycle Timing Chart



Note) 1. Shaded sections denote areas where the level can be either high or low.

2. Output load : 1TTL + 100pF

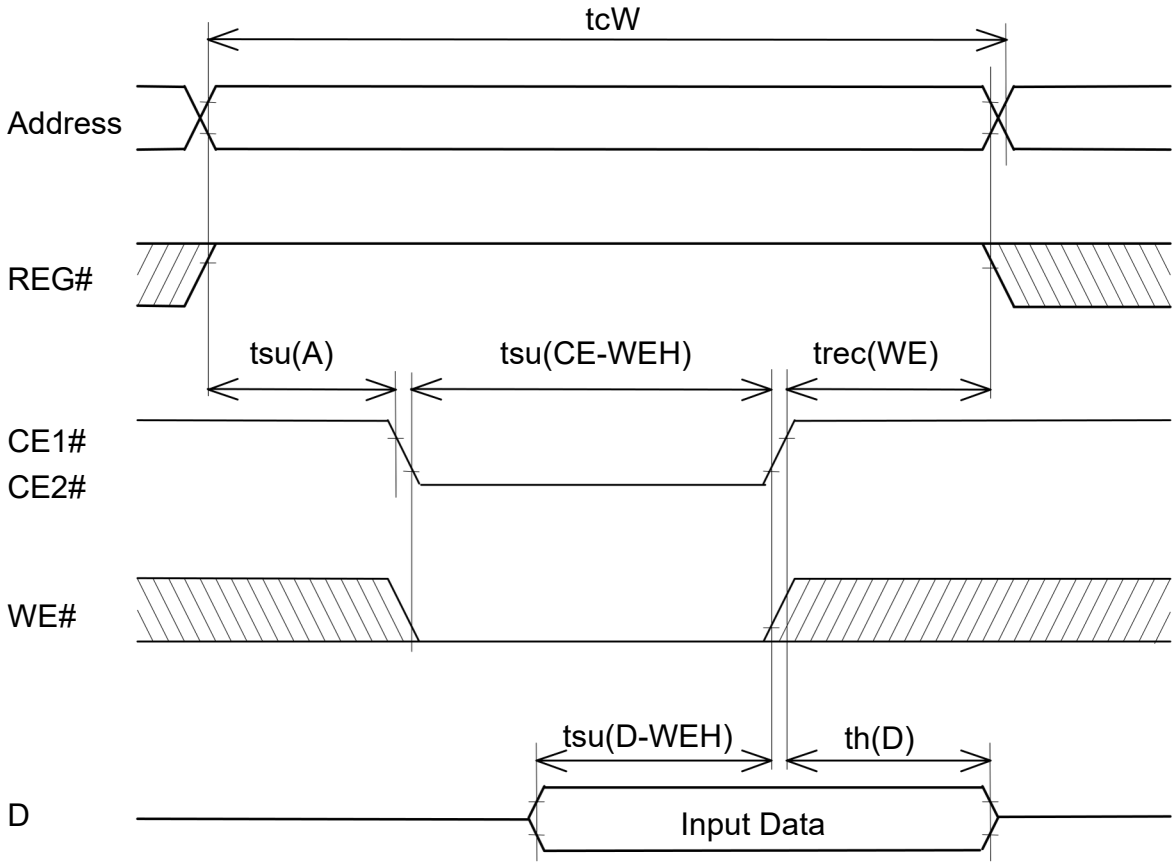
Figure 2 Attribute Memory Read Cycle timing Chart

9.2. Common memory Write Cycle Timing

Table 15 Common memory Write Cycle Timing

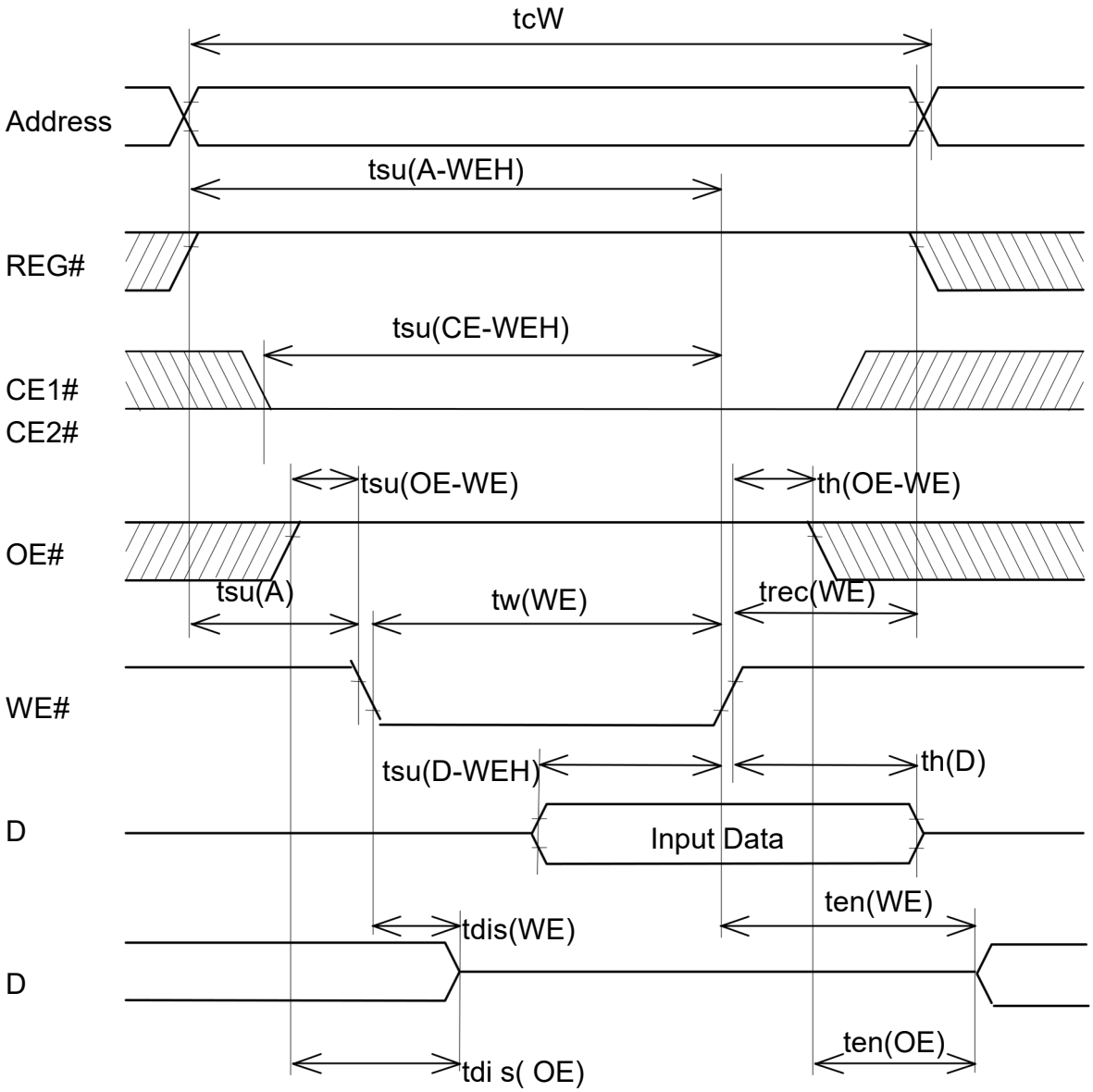
VCC=5V±10%, Ta=0℃～60℃

Parameter	Symbol	Min.	Typ.	Max.	Unit
WriteCycleTime	tCW	200			ns
WritePulseWidth	tw(WE)	120			ns
AddressSet-upTime	tsu(A)	20			ns
AddressSet-upTimefromWE#Change	tsu(A-WEH)	140			ns
CE#Set-upTimefromWE#Change	tsu(CE-WEH)	140			ns
DataSet-upTimefromWE#Change	tsu(D)	60			ns
DataHoldTime	th(D)	30			ns
WriteRecoveryTime	trec(WE)	30			ns
Output Disable Time from OE#	tdis(OE)			90	ns
OutputDisableTimefromCE#	tdis(CE)			90	ns
Output Enable Time from WE#	ten(WE)	5			ns
Output Enable Time from OE#	ten(OE)	5			ns
OE# Set-up Time from WE#	tsu(OE-WE)	10			ns
OE# Hold Time from WE#	th(OE-WE)	10			ns



Note:*1 Shaded sections denote areas where the input level can be either High or Low.
*2 When the data I/O signal is in output mode, input signal should not be applied to the card.

Figure 3 CE# Contoroled Common Memory Write Cycle timing Chart



Note: *1 Shaded sections denote areas where the input level can be either High or Low.
*2 When the data I/O signal is in output mode, input signal should not be applied to the card.

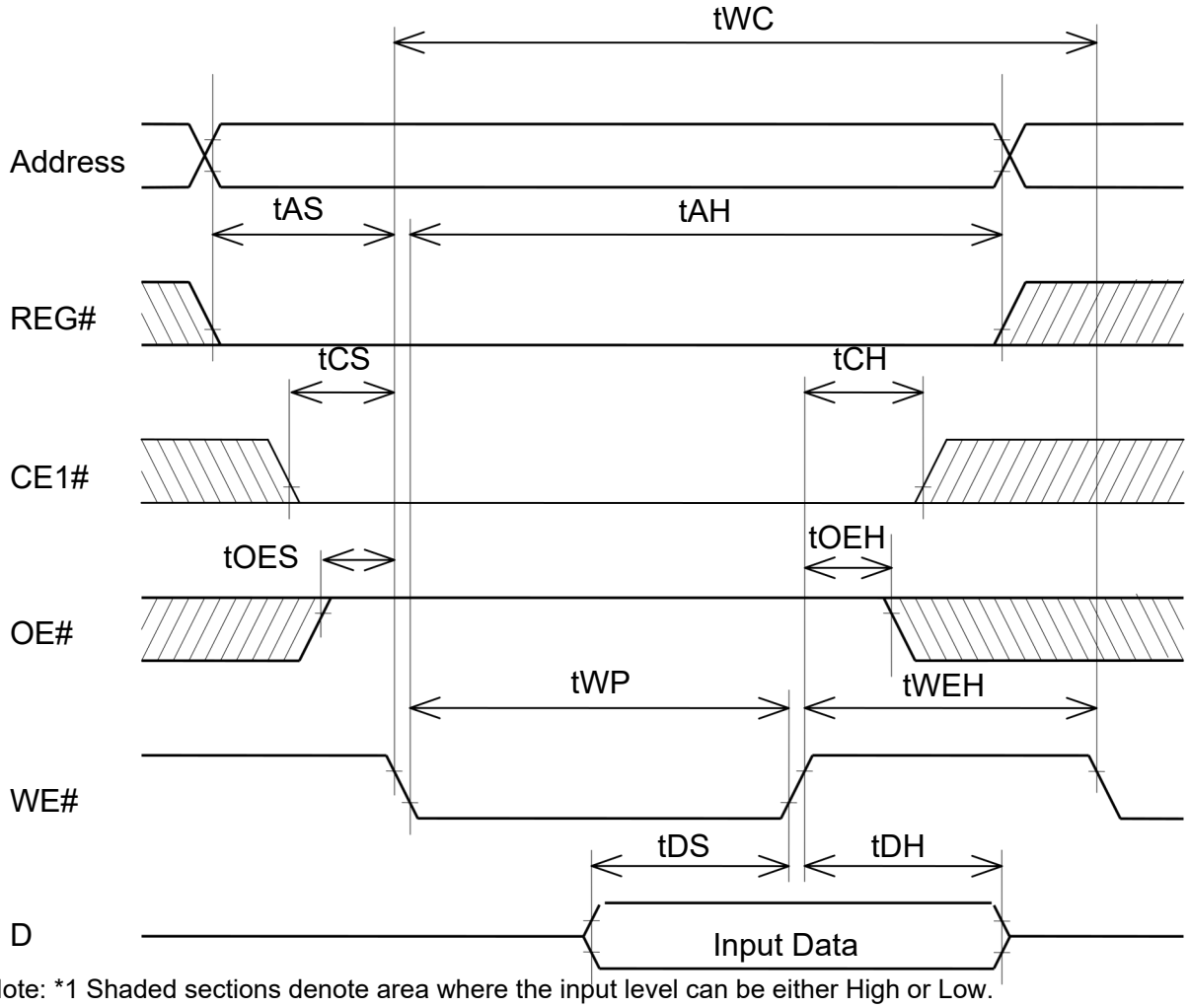
Figure 4 WE# Controlled Common Memory Write Cycle timing Chart

9.3. Attribute Memory Write Timing

Table 16 Attribute Memory Write Timing

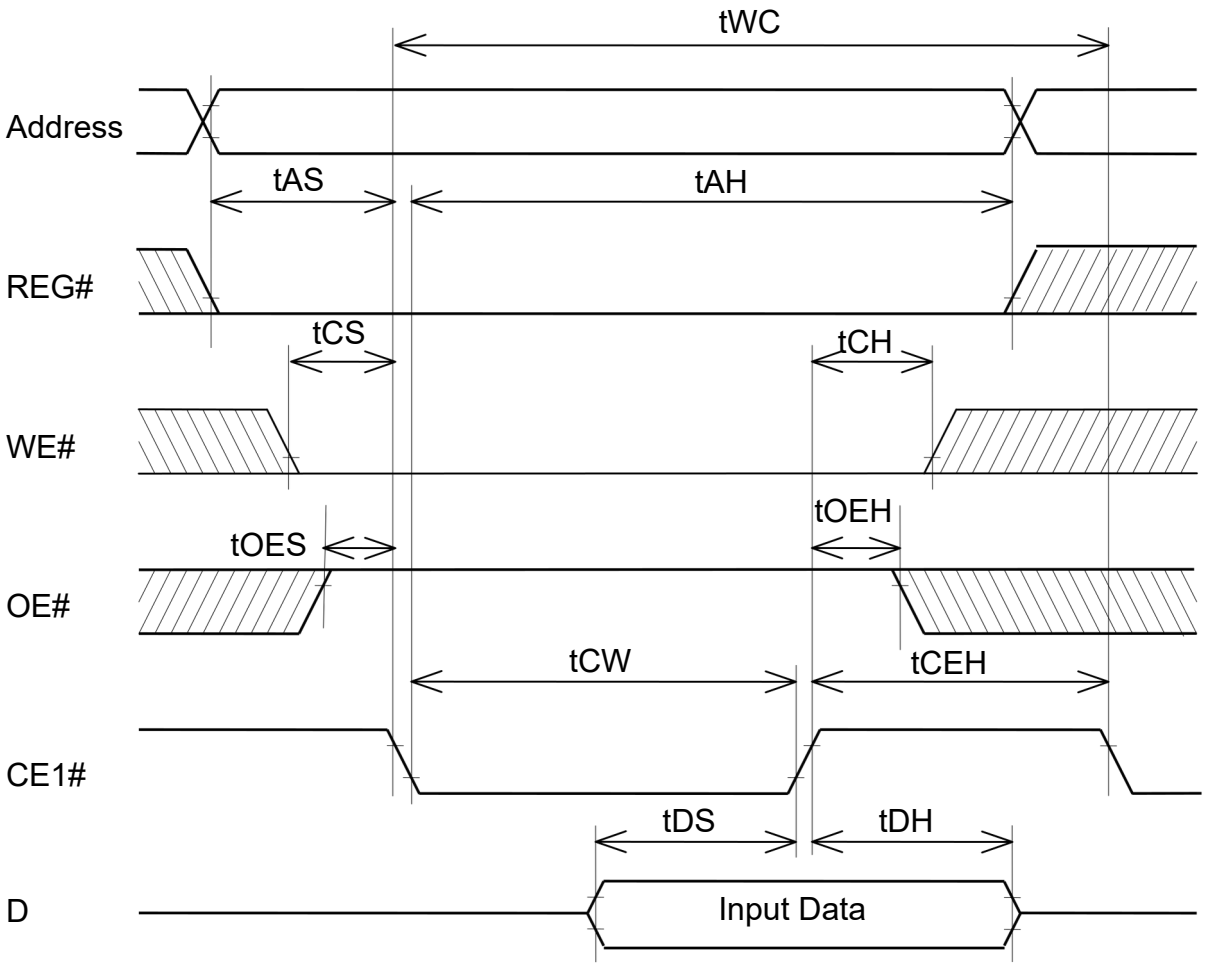
VCC=5V±10%, Ta=0℃-60℃

Parameter	Symbol	Min.	Typ.	Max.	Unit
Write Cycle Time	tWC	1.0			ms
Address Set-up Time	tAS	10			ns
Address Hold Time	tAH	100			ns
CE# Set-up Time	tCS	20			ns
CE# Hold Time	tCH	20			ns
CE# Write Pulse Width	tCW	100			ns
OE# Set-up Time	tOES	15			ns
OE# Hold Time	tOEH	30			ns
WE# Write Pulse Width	tWP	100			ns
WE# Write High Pulse Width	tWEH	0.9			ms
CE# Write High Pulse Width	tCEH	0.9			ms
Data Set-up Time	tDS	100			ns
Data Hold Time	tDH	20			ns



Note: *1 Shaded sections denote area where the input level can be either High or Low.
*2 When the data I/O signal is in output mode, input signal should not be applied to the card.

Figure 5 WE# Controlled Attribute Memory Write Cycle timing Chart



Note:*1 Shaded sections denote area where the input level can be either High or Low.
*2 When the data I/O signal is in output mode, input signal should not be applied to the card.

Figure 6 CE# Controlled Attribute Memory Write Cycle timing Chart

10. Power-up and down Sequence

10.1. Power-up and down Timing

Table 17 Power-up and down Timing

VCC=5.0V±10%, Ta=0℃～60℃

Parameter	Symbol	Test Condition	Value		Unit
			Min.	Max.	
CE# Set-up Time from VCC	tsu(VCC-CEL)		20		ms
CE# Recovery Time from VCC	trec(CEH-VCC)		1.0		μs
VCC Rising Time	tpr	from 0.1VCC to 0.9(VCC+5%)	0.1	300	ms
VCC Falling Time	tpf	from 0.9(VCC-5%) to 0.1VCC	3.0	300	ms

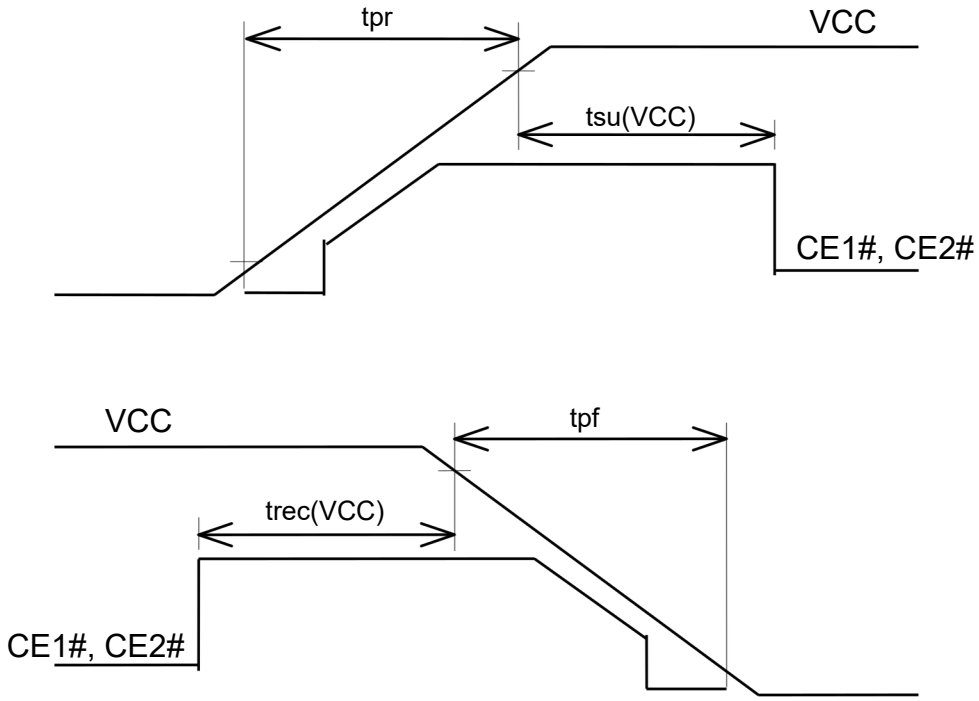


Figure 7 Power-up and down Timing

10.2. Status Output Timing

Table18 Status OutputTiming

VCC=5.0V±10%, Ta=0℃～60℃

Parameter	Symbol	TestCondition	Value		Unit
			Typ.	Max.	
BVD Output Delay Time	tBVD		6	13	ms
WP Output Delay Time	tWPO		6	13	ms

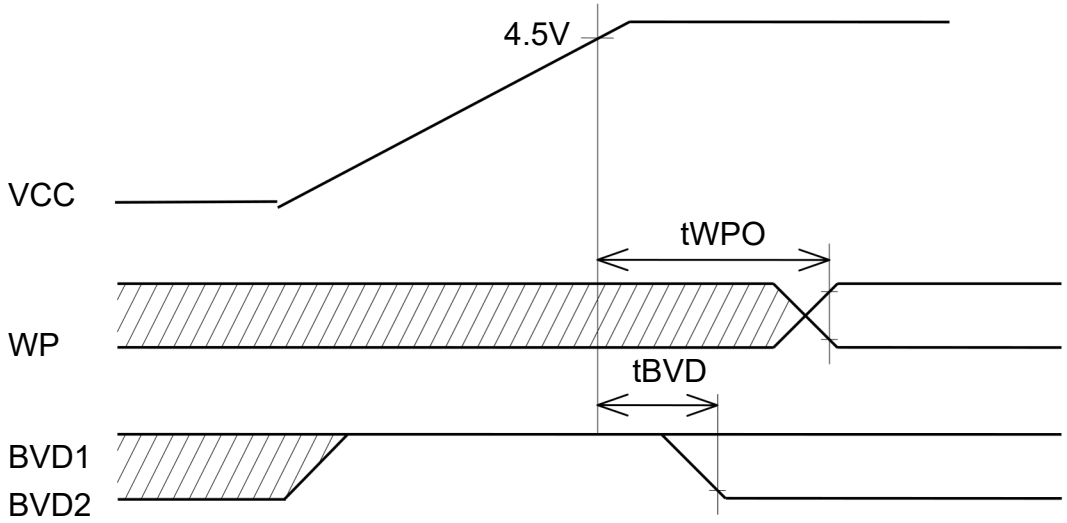


Figure 8 Status Output Timing

11. Electrical Interface

Table 19 Electrical Interface

Signal Type	Memory Size	Signal	Electrical Interface
Control Signals		CE1#	Pulled-up 20KΩ to VCC
		CE2#	Pulled-up 20KΩ to VCC
		REG#	Pulled-up 20KΩ to VCC
		OE#	Pulled-up 20KΩ to VCC
		WE#	Pulled-up 20KΩ to VCC
		RESET	NC*1
Address Signals	64KB	A[0:15]	No Resistor*2
		A[16:25]	NC
	128KB	A[0:16]	No Resistor
		A[17:25]	NC
	256KB	A[0:17]	No Resistor
		A[18:25]	NC
	512KB	A[0:17]	No Resistor
		A[18]	Pulled-down 100KΩ to GND
		A[19:25]	NC
	1MB	A[0:19]	No Resistor
		A[20:25]	NC
	2MB	A[0:19]	No Resistor
		A[20]	Pulled-down 100KΩ to GND
		A[21:25]	NC
	4MB	A[0:19]	No Resistor
		A[20,21]	Pulled-down 100KΩ to GND
		A[22:25]	NC
	8MB	A[0:20]	No Resistor
		A[21:22]	Pulled-down 100KΩ to GND
		A[23:25]	NC
		D[0:15]	No Resistor
Data Signals		BVD1	No Resistor
Output Signals		BVD2	No Resistor
		READY	NC
		WP	No Resistor
		WAIT#	NC
		CD1#	GND Level
		CD2#	GND Level
		VPP1	NC
Peripheral Power Supply		VPP2	NC

Note *1 NC stands for Not Connected with any circuitry in the card.
*2 “No Resistor” means signal is directly connected with circuitry in the card

12. Card Information Structure

BN-HSRC type in this series includes some Card Information structure (CIS) at the shipment which shares just 6 byte on 2 Kbyte attribute memory plane. This content is as follows. It's possible for user to store favorite CIS by additional writing because of EEPROM device as attribute memory. Please refer to electrical specification considering attribute memory.

Address	Data	Symbol	Description
00h	01h	***CISTPL_DEVICE_C***	***Common Memory Device Information Tuple***
02h	03h	TPL_LINK	
04h	62h	DTYPE_SRAM, DSPEED_200NS	SRAM, 200ns, WP flag Available
06h	0Bh		64KB
	1Bh		128KB
	3Bh		256KB
	7Bh		512KB
	FBh		1MB
	1Dh		2MB
	3Dh		4MB
	7Dh		8MB
08h	FFh		End of Common Memory Device Info Tuple
0Ah	FFh	***CISTPL_END***	***End of Tuple List***

13. Block Diagram

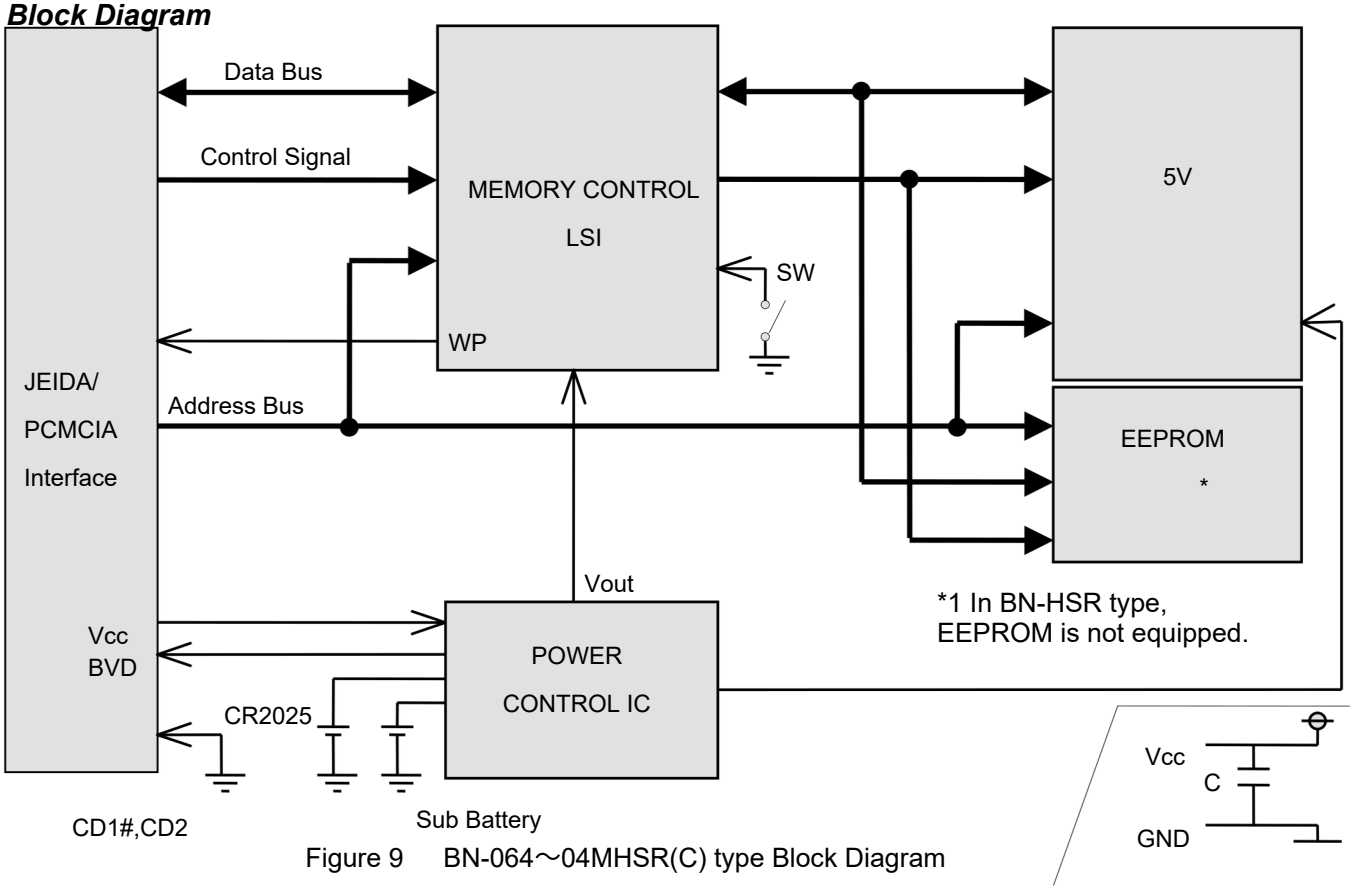


Figure 9 BN-064～04MHSR(C) type Block Diagram

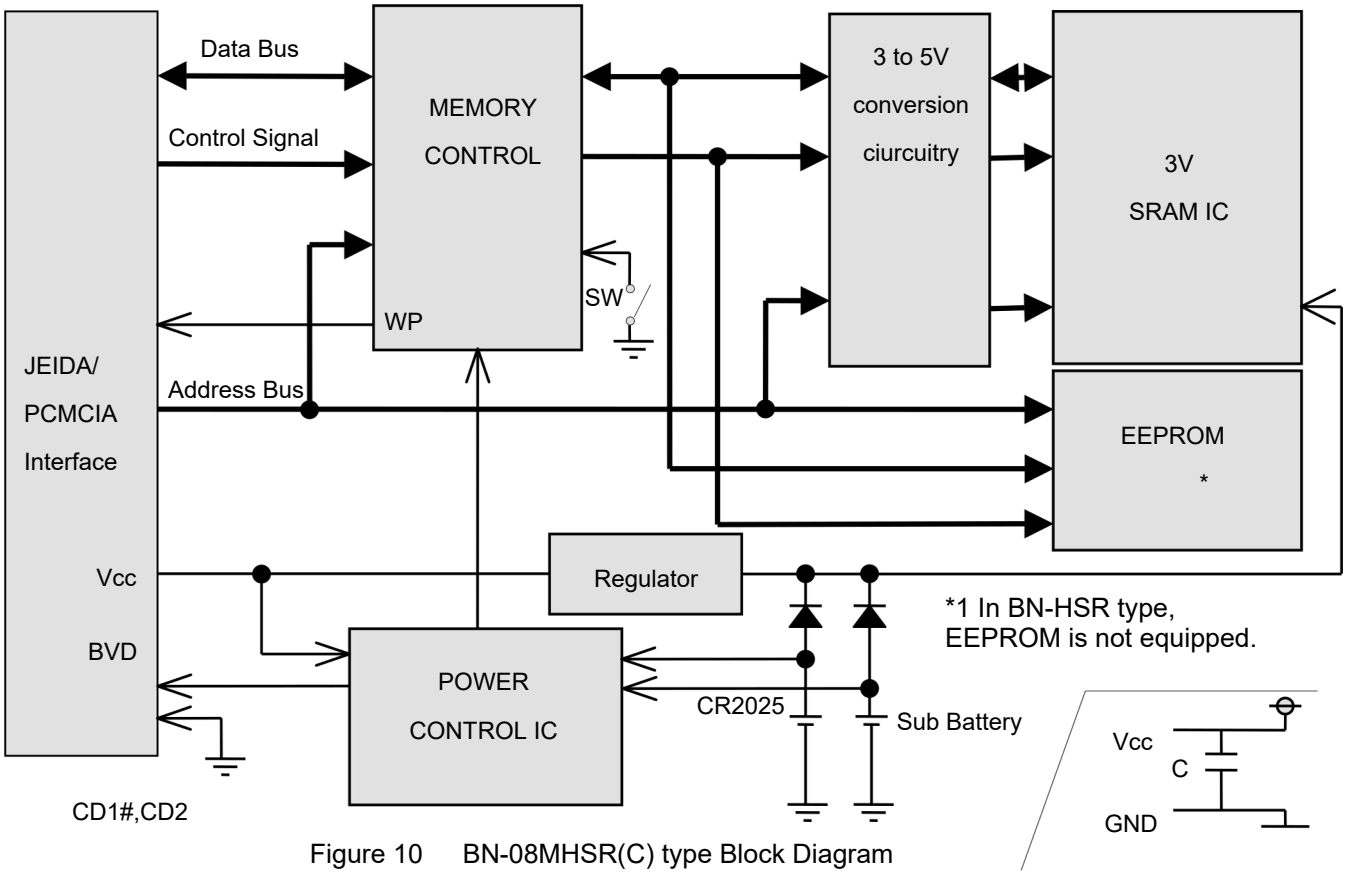


Figure 10 BN-08MHSR(C) type Block Diagram

14. Battery

14.1. Data Retention

Table 21 Data Retention

Memory Size	Memory Back-up time
	Ta=25℃
64Kbyte	5 years
128Kbyte	5 years
256Kbyte	5 years
512Kbyte	5 years
1Mbyte	5 years
2Mbyte	3 years
4Mbyte	1 years
8Mbyte	0.5 years

Note:*1 CR2025 battery produced by Panasonic should be used for main back-up battery of this card.
*2 These values are estimated back-up time when Panasonic CR2025 is used for back-up.

14.2. Battery Voltage Detection

Table 22 Battery Voltage Detection

BVD1(#63)	BVD2(#62)	Definition
H	H	Battery Operational
H	L	Battery Operational, but battery should be replaced.
L	H	Not available data retention, battery should be replaced.
L	L	Not available data retention, battery should be replaced.

Note: “H” and “L” in the table indicate High and Low Output Level each other.

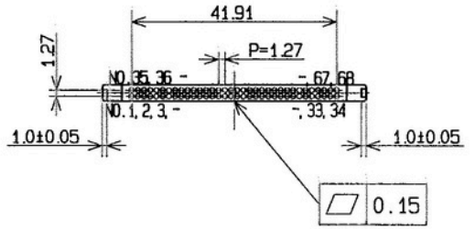
14.3. Battery Replacement

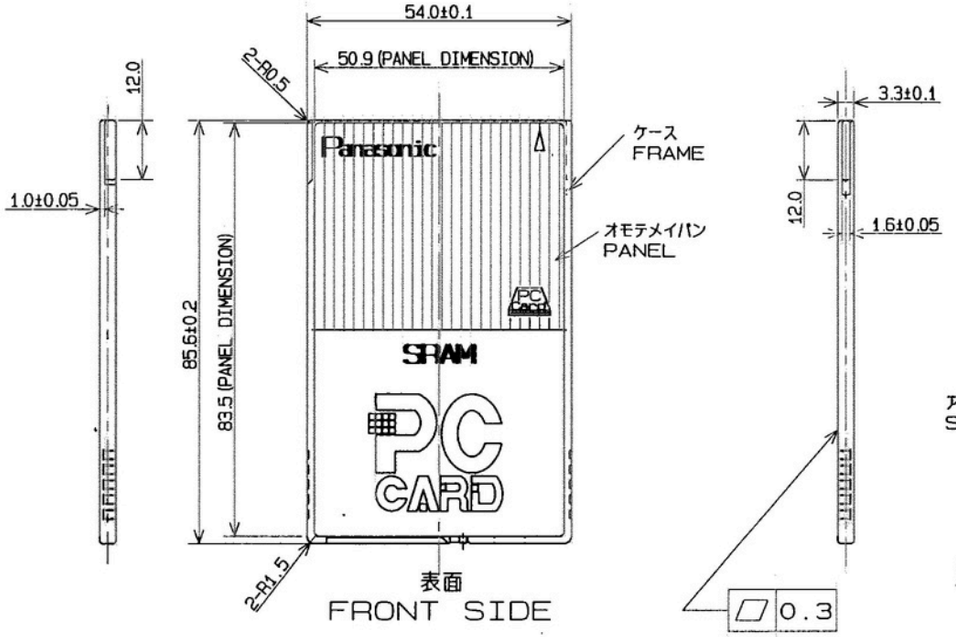
This card also includes Sub Battery which becomes back-up battery during replacement of main battery CR2025. It’s possible to replace new CR2025 within approximately 1 hour without external power supply

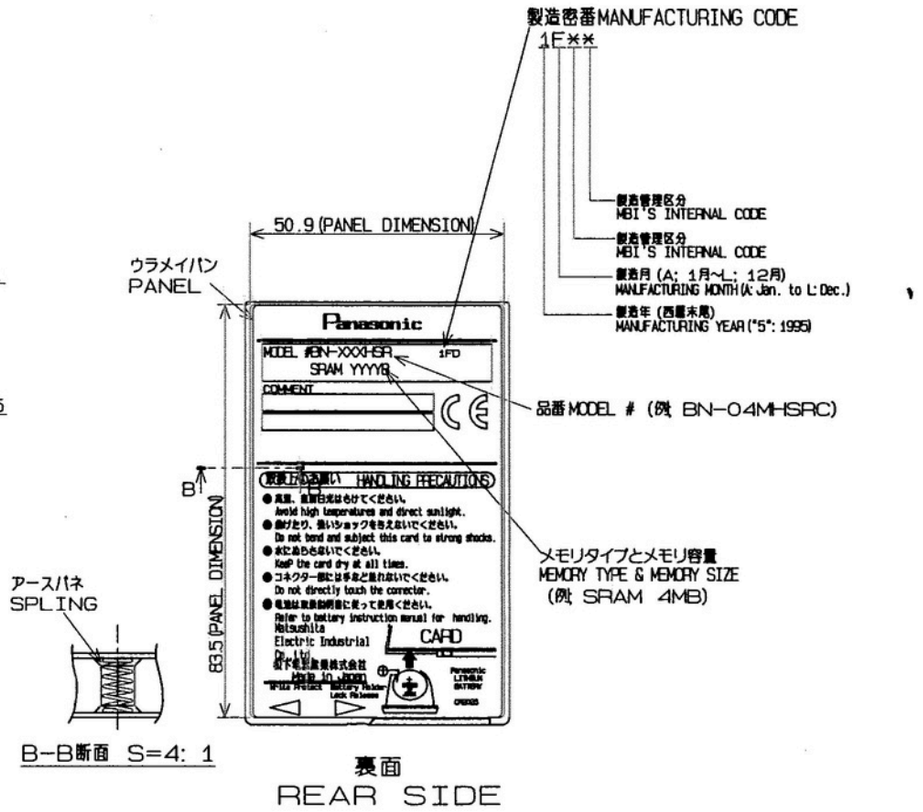
Revision History						
Rev. #	Chapter #	Title	Revision Contents		Date	
			Previous	Updated		
1					6/9/95	Nezu
1.01	8. 8.1 9. 10. 12.	DC Characteristic Stand-by Current 2mA(typ.) , 3mA(Max.) when sub-battery is full-charged AC Characteristic Power-up & down Block Diagram		100µA(typ.) , 150µA(Max.) when sub-battery is full-charged Drawn new	7/21/95	Nezu
1.1				Add BN-HSRC type	9/8/95	Nezu
				Add 4Mbyte SRAM		
	11.	Electrical Interface	512K to 2Mbyte A18 is pulled-down by 100KΩ resistor.	512K to 2Mbyte A18 is directly connec-ted with memory chip without pulled-down resistor.		
	12.	CIS		Add CIS table		
	14.1	Data Retention	5 years for 1MB 3 years for 2MB	4 years for 1MB 2 years for 2MB		
1.2				Add 64K and 128K byte SRAM	11/17/95	Nezu
	10.2	Status Output Timing	tBVD=10µs(Typ.)	tBVD=10ms(Typ.)		
2.0	10.2	Status Output Timing	tBVD=10ms(Typ.) tWPD=1.5ms(Typ.) =2.0mS(Max.)	tBVD=6ms(Typ.) =13ms(Max.) tWPD=6ms(Typ.) =13mS(Max.)	10/31/96	Toyokuni
2.0	11	Electrical Interface for Address Signal 128Kbyte A16 : 512Kbyte : A18 : 1Mbyte : A19 : 2Mbyte A19 4Mbyte A19	 Pulled-down 100KΩ to GND No Resistor Pulled-down 100KΩ to GND Pulled-down 100KΩ to GND Pulled-down 100KΩ to GND	 No Resistor Pulled-down 100KΩ to GND No Resistor No Resistor No Resistor	10/31/96	Toyokuni
2.1	13.1	Data Retention 1Mbyte : 2Mbyte :	 4years 2years	 5years 3years	5/29/97	Toyokuni
2.2	2,11,13	Add Model# BN-08MHSR(C)			7/9/97	Toyokuni

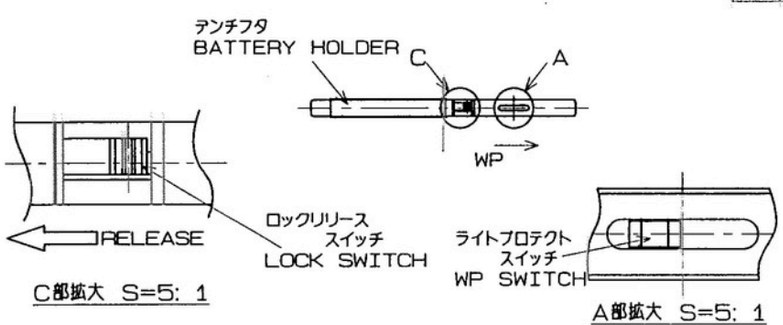
Revision History						
Rev. #	Chapter #	Title	Revision Contents		Date	
			Previous	Updated		
3.0	11	Electrical Interface for Address Signal 2Mbyte A20 : 4Mbyte A20 8Mbyte A19,A20 :	 Pulled-down 100KΩ to GND Pulled-down 100KΩ to GND Pulled-down 100KΩ to GND	 No Resistor No Resistor No Resistor	9/17/01	Toyokuni
	13	Block Diagram (BN-02MHSR(C) ～BN-08MHSRC)	Configured by 5V-SRAM IC	Configured by 3V-SRAM IC w/ 3 to 5V conversion ciurcuitry		
3.1	11	Electrical Interface for Address Signal 2Mbyte A20 : 4Mbyte A20	 No Resistor No Resistor	 Pulled-down 100KΩ to GND Pulled-down 100KΩ to GND	7/22/03	Toyokuni
	13	Block Diagram (BN-02MHSR(C) ～BN-04MHSRC)	Configured by 3V-SRAM IC w/ 3 to 5V conversion ciurcuitry	Configured by 5V-SRAM IC		

Sym.	Date	Revision	Signed	Checked









D.	C.						
	E.	Item or No.	Material & Size	qt.	S.P qt	Process & Finishing	
Nominal Size	v.t	Nominal Size	v.t	Jap. Name			
				Eng. Name	CARD OUTSIDE DRAWING		
Scale 1: 1	Designed K.Toyokuni 18-06-01	Drawn K.Toyokuni 18-06-01	Traced	Checked	Approved	M No	A No	F. No

A3 MATSUSHITA BATTERY INDUSTRIAL CO., LTD. 3rd Angle System Unit: mm

T&O ELECTRONIC SOLUTIONS