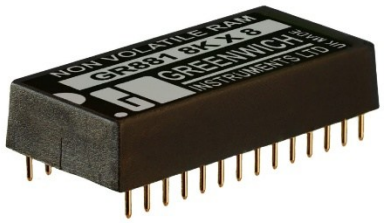
NON-VOLATILE RAM
GR881 (8k X 8)

T&O ELECTRONIC SOLUTIONS

August 2025



Description

The GR881 is a 8192 word by 8 bits (8k x 8) non-volatile, advanced silicon gate, CMOS 70nS Static RAM IC with a high operational industrial temperature range. Memory contents are retained by the use of an internal, highly reliable, lithium power cell. Without any external power, the data retention is typically greater than ten years.

The pin-out of the device conforms to the JEDEC standards and is fully compatible with normal Static RAM. The power down circuit is fully automatic and is referenced at 4.5Vdc. At this point it is write-protected by an internal inhibit function for data protection and the memory contents are retained by the internal lithium cell.

Essential for data integrity, power down is very fast, less than 15µS from 5V to 0Vdc, faster than system power failure conditions.

Application

When powered down, the device is transportable and the data contained can be moved from system to system making it ideal for program development, data collection in data-loggers, program changes in process control systems, automation and user-definable lookup tables etc.

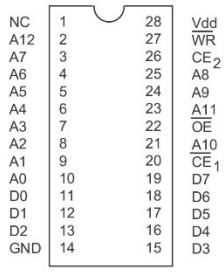
Absolute Ratings

SYMBOL	MIN	MAX	UNITS
Vdd	-0.3	7.0	Vdc
Vin/out	-0.3	Vdd+0.3	Vdc
Temp	-40	+85	°C

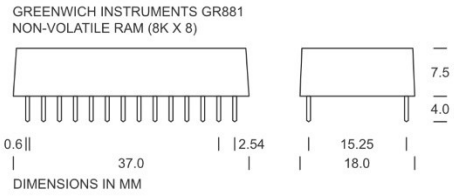
Operating Conditions

SYMBOL	MIN	TYP.	MAX	UNITS
Vdd	+4.75	+5.0	+5.5	Vdc
Vin(1)	+2.2		Vdd+0.3	Vdc
Vin(0)	-0.3		+0.8	Vdc
Iin (any other pin)	-1.0		+1.0	µA
Vout(1) (Iout=-1mA)	+2.4			Vdc
Vout(0) (Iout=+2mA)			+0.4	Vdc
Idd(active)		30		mA
Idd(deselected)		1.0		mA
Tcycle			70	nS
Cin(any pin)		10		pF

Pin Connections



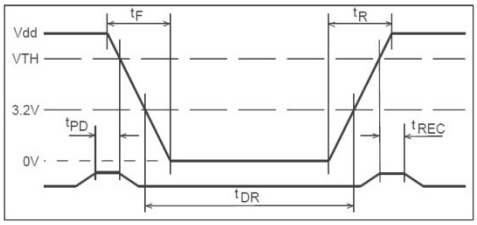
Pin	Function
A0-A12	Address I/P`s
D0-D7	Data in/out
OE	Output Enable
CE1 CE2	Chip Enable
WR	Write Enable
Vdd	+5Volt Power
GND	Ground



Operating Mode

CE	OE	WR	MODE	OUTPUT	Idd
H	X	X	Unsel.	Hi-Z	Standby
L	H	H	Unsel.	Hi-Z	Active
L	L	H	Read	Dout	Active
L	X	L	Write	Din	Active

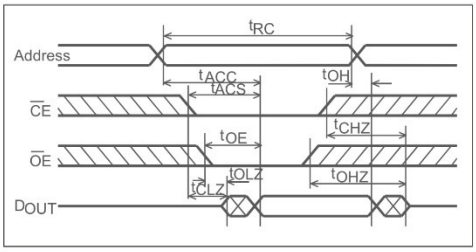
Data Retention Operating Conditions



SYM	PARAMETER	MIN	TYP.	MAX	UNITS
Vdd	Operating supply voltage	4.75	5.0	5.5	Vdc
VTH	Data retention voltage		4.5		Vdc
tF	Vdd slew to 0V	15			µS
tR	Vdd slew from 0V to 5V	15			µS
tREC	CE to O/P valid from power up			15	µS
tDR	Data retention time		10		Yrs.
tPD	CE at Vin(1) before power down	0			µS

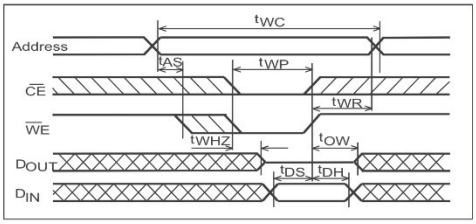
Please note:
1. WR must be high during address transitions
2. A write occurs during the overlap of active CE and a low WR
3. CE = CE1 and CE2
4. WR is high for a read cycle

Read Cycle



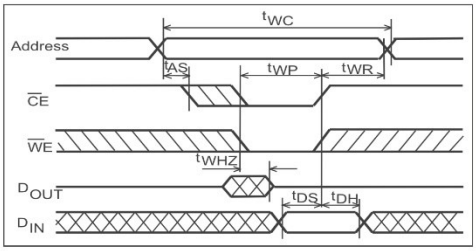
SYM	PARAMETER	MIN	MAX	UNITS
tRC	Read cycle time	70		nS
tACC	Access time		70	nS
tACS	CE to output valid		70	nS
tOE	OE to output valid		35	nS
tCLZ	CE to output active	10		nS
tOLZ	OE to output active	10		nS
tOH	Output hold time	10		nS
tCHZ	CE to output disable		25	nS
tOHZ	OE to output disable		25	nS

Write Cycle 1



SYM	PARAMETER	MIN	MAX	UNITS
tWC	Write cycle time	70		nS
tWP	Write pulse width	50		nS
tAS	Address setup time	0		nS
tWR	Write recovery time	10		nS
tWHZ	WR to output disable		20	nS
tOW	Output active from WR	5		nS
tDS	Data setup time	30		nS
tDH	Data HOLD TIME	0		nS

Write Cycle 2



TecSys by
T&O Electronic Solutions GmbH
Tiefenbachstr. 5
83734 Hausham
Germany

Tel: +49 8026 92 862 - 0
Email: sales@tecsys.de
https://shop.tecsys.de

Do not dispose of non-volatile memory devices by incineration, crushing or landfill; devices can be returned, carriage paid, to Cephos Relays Limited for disposal

RoHS Compliant